Paper No. 40

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte GUENTHER WAITL
FRANZ SCHELLHORN and
HERBERT BRUNNER

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Appeal No. 1999-0598
Application No. 08/866,064

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ON BRIEF

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Before THOMAS, KRASS, and BARRETT, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 8-15, all of the pending claims.

The invention is directed to surface mount technology (SMT). More particularly, the invention pertains to a two-pole SMT miniature housing for semiconductor components and a method of manufacturing the same.

Representative independent claim 8 is reproduced as follows:

8. A two-pole surface mount technology (SMT) miniature housing in lead frame technique for a semiconductor component and which is mountable on a printed circuit board having a flat surface, comprising:

a housing having a surface facing the printed circuit board all of which is flat, all of which is parallel to, and all of which is in contact with the printed circuit board so as to form a planar component mounting surface;

a semiconductor chip encapsulated in the housing;

a first lead frame part having the semiconductor chip mounted thereon at a chip mounting surface thereof and a second lead frame part contacted to the chip, both lead frame parts being conducted out of the housing;

the first and second lead frame parts each forming solder terminals alongside the housing, a width of the planar mounting surface being greater than a thickness of the solder terminals;

said solder terminals being formed as punched parts and which are finished solder terminals not requiring further length change and which run alongside and laterally project outwardly from sidewalls of the housing at opposite sides of the housing, said solder terminals extending vertically downwardly to a position level with and having unbent ends terminating at and even with the planar component mounting surface of the bottom of the housing so that the solder terminals can be soldered to the printed circuit board at a top surface thereof , said first and second lead frame parts with their solder terminals having no portions which are mechanically bent and thus have no bending stresses at any portions thereof; and

said chip mounting surface and said planar component mounting surface formed by said housing floor being at right angles with respect to one another.

The examiner relies on the following references:[1]

Craft	4,941,067	Jul. 10, 1990
Waitl et al. (Waitl)	5,040,868	Aug. 20, 1991
Stokes et al. (Stokes)	5,043,791	Aug. 27, 1991
Ishizaki et al. (Ishizaki)	JP 2-156,558	Jun. 15, 1990
Iwajima (Osamu)	JP 04-128,811	Apr. 30, 1992

Claims 8-15 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner cites, alternatively, Ishizaki and Stokes, or Ishizaki, Stokes and Osamu[2], with regard to independent claims 8 and 14, adding Craft with regard to claims 9 and 15, and adding Waitl to the original combinations with regard to claims 10, 12 and 13. The statement of rejection in the answer does not state what references are relied upon in rejecting claim 11.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

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[1] Our understanding of the Osamu and Ishizaki references is based on English translations thereof prepared for the United States Patent and Trademark Office. Copies of these translations are attached hereto.

[2]We will refer to this reference as "Osamu" since both appellants and the examiner refer to it that way but this appears to be the first name of the inventor. The inventor's last name appears to be Iwajima.

OPINION

At the outset, we note that claim 11 is neither part of the examiner's statement of rejection nor is it discussed in the explanation of the rejection. Similarly, appellants do not mention or discuss claim 11 in the briefs, regarding the rejection thereof. The final rejection only mentions claim 11 in regard to including it under rejection based on 35 U.S.C. § 112, a rejection apparently withdrawn in the answer. However, since claims 12 and 13 stand rejected under 35 U.S.C. § 103, and these claims depend from claim 11, we presume that claim 11 also stands rejected under 35 U.S.C. § 103 in view of the same references applied against claims 10, 12 and 13.

With regard to independent claims 8 and 14, it is the examiner's position that Ishizaki teaches a semiconductor chip 32 encapsulated in a housing 38 having a surface (the surface is identified as the edge portion at 38a formed by the line intersection of the two intersecting inclined base planes) facing the circuit board 39, "all of which is flat, all of which is parallel to , and all of which is in contact with the printed circuit board so as to form a planar component mounting surface" [answer-page 2]. The examiner also identifies a first planar lead frame part 25 and a second planar lead frame part 26 "forming solder 41 terminals 35, 37 along side the housing" [answer-page 3]. The examiner further states that Ishizaki discloses that the solder terminals are

"finished solder terminals not requiring further length change and which run alongside and laterally project outwardly from opposite sidewalls of the housing and extending vertically downward to a position level with a planar mounting surface (the edge portion at 38a) of the bottom of the housing and having unbent ends" [answer-page 3].

The examiner takes issue with the claimed term, "a width of the planar mounting surface being greater than a thickness of the solder terminals," taking the view that "a" width can be any portion of the total width of the mounting surface and "a" thickness can be any portion of the total thickness of the solder terminals. Therefore, concludes the examiner, this limitation is "inherent" in Ishizaki.

The examiner dismisses the claimed limitation of the lead frame parts being "punched parts" as a "process limitation" not further limiting the product. The examiner also dismisses the failure of Ishizaki to teach solder terminals which "can be" soldered to the printed circuit board at a top surface thereof because this is an "intended use" which does not result in a structural difference between the claimed apparatus and the apparatus of Ishizaki.

The examiner employs Stokes for a teaching of the functional and mechanical equivalency of through hole terminals and joints, and butt terminals and joints and

concludes that it would have been obvious to combine the references "because it would enable the formation of the planar component mounting surface, all of which is in contact with the printed circuit board, as taught by Ishizaki" [answer-page 5]. The examiner also concludes that Stokes teaches a product comprising solder terminals being soldered to a printed circuit board at a top surface thereof [identifying the abstract, lines 18-20, column 1, line 65 to column 2, line 14 and column 10, lines 55-58] and concludes that it would have been obvious to combine this teaching with Ishizaki "because it would facilitate bonding of the butt terminals of the combination" [answer-page 5].

For their part, appellants argue that the bottom edge 38a in Fig. 7(b) of Ishizaki is in a V-shape so that only the center line of the V contacts the board. We agree. Since this center line is not a "surface" of the housing, Ishizaki cannot meet the claim limitation of the housing surface facing the circuit board "all of which is flat, all of which is parallel to, and all of which is in contact with the printed circuit board so as to form a planar component mounting surface." The housing "surface" in Ishizaki is not "flat," as claimed.

The examiner argues this point by contending that "the scope of the claims is not limited to a product not comprising only a small portion of the surface facing the printed circuit board in contact with the printed circuit board, and the remaining upwardly sloping

portions of the surface facing the printed circuit board are not in contact with the printed circuit board and are rounded and not flat or planar" [answer-page 9]. We disagree. The claims do, in fact, require all of the housing surface facing the printed circuit board to be "flat." While one may say that the center line of the V in Ishizaki is parallel to and in contact with the printed circuit board, it is unreasonable, in our view, to contend that this center "line" constitutes a "surface," as claimed. Since Stokes is no help in overcoming this deficiency of Ishizaki, we will not sustain the rejection of claims 8 and 14 under 35 U.S.C. § 103 over the combination of Ishizaki and Stokes.

Moreover, while we understand the examiner's creative argument that "a" width of the planar mounting surface may comprise less than the total width and that "a" thickness" of the solder terminals may comprise less than the total thickness, we do not agree with it. It is our view that it is simply unreasonable, especially in view of the instant specification, to treat the claim recitation of "a width of the planar mounting surface being greater than a thickness of the solder terminals" as meaning anything other than that the total width of the planar mounting surface is greater than the total thickness of the solder terminals.

We also agree with appellants that Fig. 7(b) of Ishizaki clearly shows that the solder terminals extend through and beyond the bottom portion of the circuit board 39. Therefore, Ishizaki cannot suggest the claimed limitation of solder terminals having "ends terminating

at and even with the planar component mounting surface..." While the examiner recognizes this, Stokes is relied on for a teaching of the equivalency of through hole terminals and butt terminals and concludes that the through hole terminals of Ishizaki may obviously be butt terminals. The examiner states that the combination of Ishizaki and Stokes would have been made "to facilitate mounting," but we find nothing to support such an argument and no cogent reason why the skilled artisan would have substituted butt terminals for the through hole terminals disclosed by Ishizaki.

For at least the reasons supra, we will not sustain the rejection of independent claims 8 and 14 under 35 U.S.C. § 103 over Ishizaki and Stokes.

The examiner makes an alternative rejection of these claims under 35 U.S.C. § 103 based on the addition of Osamu to the combination of Ishizaki and Stokes.

We will not sustain this alternative rejection since, in our view, Osamu does not provide for the deficiencies noted supra with regard to Ishizaki and Stokes. More particularly, the examiner relies on Osamu to provide for a teaching of "a width of the planar mounting surface being greater than a thickness of the solder terminals," as claimed, even if our interpretation of this claim language, supra, is accepted.

Even assuming, arguendo, that the examiner's argument has merit, and Osamu does teach the width of a planar mounting surface to be greater than a thickness of the solder terminals, this still does not provide for the claim limitation of the solder terminals

having “ends terminating at and even with the planar component mounting surface...” And, for the reasons supra, the combination of Ishizaki and Stokes does not make this claimed subject matter obvious.

Moreover, even assuming, arguendo, that the examiner’s argument has merit, and Osamu does teach the width of a planar mounting surface to be greater than a thickness of the solder terminals, this still does not provide for the claim limitation of the housing surface facing the circuit board “all of which is flat, all of which is parallel to, and all of which is in contact with the printed circuit board so as to form a planar component mounting surface.” The housing “surface” in Ishizaki is not “flat,” as explained supra, and Osamu does not clearly provide for this deficiency. As seen in Osamu, in Figure 2, it is unclear what the bottom of resin mold 111 looks like, or whether it is a flat surface at all. Looking at Figures 1 and 5, the top of the resin mold appears to be made up of angled surfaces, with an uppermost surface being flat but not the same width as the overall width of the resin mold. One might say that this thinner surface is still a flat surface, as claimed. However, we would need to speculate in order to determine that the bottom of the resin mold contacting the substrate is also such a flat surface. It is not clear from Osamu’s disclosure. Moreover, even if we determined that Osamu disclosed such a surface, Osamu’s lead terminals do not stop at the surface of the

substrate but are extended through the surface. The only reference which could possibly suggest the solder terminals, as claimed (i.e., "terminating at and even with the planar component mounting surface of the bottom of the housing") would be Stokes. Yet, notwithstanding the examiner's explanation that Stokes teaches that

stopping the terminals at the surface of the circuit board or extending the terminals through the circuit board are obvious alternatives, we find no reason for the skilled

artisan to have modified either Ishizaki or Osamu so as to omit the through holes therein and use, in their place, solder terminals which terminate at and even with the planar component mounting surface of the bottom of the housing.

Since we have not sustained the rejection of independent claims 8 and 14 under 35 U.S.C. § 103, we also will not sustain the rejection of dependent claims 9-13 and 15 under 35 U.S.C. § 103 since the references to Craft and Waitl, employed against varying claims in one capacity or another, do not provide for the deficiencies of the primary references.

The examiner's decision rejecting claims 8-15 under 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)))))) BOARD OF PATENT
ERROL A. KRASS Administrative Patent Judge	) APPEALS) AND) INTERFERENCES
LEE E. BARRETT Administrative Patent Judge	))))

eak/vsh

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